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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,652	03/02/2004	Hiroyuki Ogiso	9319S-000694	2704

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/791,652	OGISO ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6 and 8* is/are rejected.

7)☒ Claim(s) *2,3 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 8/3/05 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections, and therefore, these are withdrawn. However, the prior art rejections are remained and repeated for the reasons set forth below. This action is FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,260,979, issued to Parker et al. in view of US Pat. 5,477,330, issued to Dorr.

As per claim 1, Parker discloses a clock shaping device (figure 1), provided in a transmission apparatus and compensating for network synchronization (this limitation is merely an intended use of the device, therefore, no patentable weight is given accordingly), for receiving an input of a back-up clock signal (REFCLK2) in sync with a reference clock signal from a master station and supplied from a clock supply apparatus and an input of reception data from a transmission path (where the clock signal REFCLK2 comes from is merely an intended use of the device, therefore, no patentable weight is given accordingly), and generating a reception

clock signal (REFCLK1) through timing-extraction from said reception data, said device comprising:

a first clock signal selection portion (a portion of the MUX 12 which receives clock signals REFCLK1 and REFCLK2) that receives an input of said reception clock signal (REFCLK1) and an input of said back-up clock signal (REFCLK2), selects either of said clock signals by a first selection signal (REFCLK1_ACTIVE, REFCLK2_ACTIVE) inputted from outside (SELECTOR 14 is outside of the MUX 12), monitors, when said reception clock signal is being selected, a loss in said selected reception clock signal, and switches said selected reception clock signal to said back-up clock signal upon detection of said loss (the recited functions are explicitly disclosed in column 4, lines 49-58, i.e., the REFCLK1 clock signal is monitored. If the REFCLK1 is invalid, select the REFCLK2 clock signal);

an oscillation circuit (figure 4, RC oscillator 104) that oscillates at a predetermined frequency;

a second clock signal selection portion (the portion of the MUX 12 which receives one of the clock signals REFCLK1, REFCLK2 and the RC_CLK clock signal) that receives an input of a clock signal from said first clock signal selection portion (either the clock signal REFCLK1 or REFCLK2) and an input of a clock signal (RC_CLK) from said oscillation circuit (RC oscillator 104), selects either of said clock signals by a second selection signal (RC_CLK_ACTIVE) inputted from outside, monitors, when said back-up clock signal is being selected, a loss in said selected back-up clock signal, and switches said back-up clock signal to said clock signal from said oscillation circuit upon detection of said loss (the recited functions are explicitly disclosed in

column 4, lines 56-60, i.e., if the clock signals REFCLK1 and REFCLK2 are invalid, select the RC_CLK clock signal);

a voltage controlled oscillation circuit (the combination of VCO 24 and dividers 30 and 32) having a frequency that varies with a control voltage being supplied (this is a standard function of a VCO), and generates and outputs a feedback loop output signal (the signal at the output of divider 30);

a phase comparison portion (PHASE DETECTOR 16) that generates a phase difference signal based on a result of comparing said feedback loop output signal from said voltage controlled oscillation circuit and a clock signal outputted from said second clock signal selection portion (as shown, REFCLK is compared with OSCOUT); and

a loop filter (LOOP FILTER 22) that smoothes said phase difference signal and outputs said phase difference signal in the form of said control voltage.

wherein the voltage controlled oscillation circuit includes a forward feedback oscillation loop circuit (dividers 30 and 32) that outputs said feedback loop output signal (the signal at the output of divider 30) and a forward feedback oscillation loop output signal (the signal at the output of divider 32).

Parker does not explicitly disclose the oscillation circuit 104 is a quartz crystal oscillator as called for in the claim.

Dorr explicitly discloses in the abstract that an oscillator circuit implemented using quartz crystal would provide highly accurate and stable frequency signal.

It would have been obvious to one skilled in the art at the time of the invention was made to replace the Parker's RC oscillator by a quartz crystal oscillator circuit for the advantage discussed herein above.

As per claim 4, Parker further discloses:

a first selection portion (figure 1, a portion of MUX 12 which receives REFCLK1 and REFCLK2) that receives an input of said reception clock signal and an input of said back-up clock signal, and selects and outputs either of said clock signals by said first selection signal;

a reception clock signal loss detection portion (figure 4, VALID REFCLK1 DETECTOR 98) that detects a loss in said reception clock signal when said reception clock signal is being selected in said first selection portion, and outputs said detection to said first selection portion in the form of a first switching signal (REFCLK1_FAIL), and

wherein said first clock signal selection portion switches said reception clock signal to said back-up clock signal by said first switching signal given with precedence over said first selection signal (column 4, lines 49-58).

As per claim 5, Parker further discloses:

a second selection portion (figure 1, a portion of MUX 12 which receives REFCLK2 and RC_CLK) that receives an input of a clock signal outputted from said first clock signal selection portion and an input of a clock signal outputted from said quartz crystal oscillation circuit, and selects and outputs either of said clock signals by said second selection signal; and

a back-up clock signal loss detection portion (figure 4, VALID REFCLK2 DETECTOR 102) that detects a loss in said back-up clock signal when said back-up clock signal is being

selected in said second selection portion, and outputs said detection to said second selection portion in the form of a second switching signal (REFCLK2_FAIL), and

wherein said second clock signal selection portion switches said back-up clock signal to said clock signal from said quartz crystal oscillation circuit by said second switching signal given with precedence over said second selection signal (column 4, lines 56-60).

As per claim 6, Parker discloses a device having the structure discussed in claim 1 but he does not explicitly disclose first and second dividing means connected as recited in the claim.

The examiner takes Official Notice the fact that the practice of dividing the frequency of the reference signal and dividing the frequency of the feedback signal in a PLL circuit to reduce the frequency of these operating signals is well-known.

It would have been obvious to one skilled in the art at the time of the invention was made to insert first and second dividing means to the Parker's PLL circuit to reduce the frequency of the reference signal and the frequency of the feedback signal. The motivation and/or suggestion would be to allow the Parker's PLL to be able to function in applications which operate with very high frequency signals.

As per claim 8, this claim is rejected for the same reasons and motivation discussed in claim 1. The recited limitation "electronic instrument" is met because the Parker's PLL circuit is obviously used to provide clock for an electronic instrument.

Response to Arguments

3. Applicant's arguments filed on 8/3/05 have been fully considered but they are not persuasive.

Regarding the argument that Parker does not disclose or suggest a VCO which includes a forward feedback oscillation loop circuit that outputs said feedback loop output signal and a forward feedback oscillation loop output signal as recited in claim 1.

As discussed in the preceding rejection, the VCO (the combination of VCO 24 and dividers 30 and 32) includes a forward feedback oscillation loop circuit (dividers 30 and 32) that outputs said feedback loop output signal (the signal at the output of divider 30) and a forward feedback oscillation loop output signal (the signal at the output of divider 32).

Allowable Subject Matter

4. Claims 2-3 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

These claims are allowed for the reasons noted in the previous Office action.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/27/05

Minh Nguyen
Primary Examiner
Art Unit 2816